AN ELECTRONICALLY TUNABLE FREQUENCY SYNTHESIZER DESIGN FOR AN UHF RECEIVER

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THESIS

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by

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December 1979

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REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) An Electronically Tunable Frequency Synthesizer Design for an UHF Receiver		5. TYPE OF REPORT & PERIOD COVERED Master's Thesis; December 1979 6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s) Cuneyt Bilgihan		8. CONTRACT OR GRANT NUMBER(s)
9. PERFORMING ORGANIZATION NAME AND ADDRESS Naval Postgraduate School Monterey, California 93940		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
11. CONTROLLING OFFICE NAME AND ADDRESS Naval Postgraduate School Monterey, California 93940		12. REPORT DATE December 1979 13. NUMBER OF PAGES 57
14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office)		15. SECURITY CLASS. (of this report) Unclassified 15a. DECLASSIFICATION/DOWNGRADING SCHEDULE
16. DISTRIBUTION STATEMENT (of this Report) Special Distribution		
17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)		
18. SUPPLEMENTARY NOTES		
19. KEY WORDS (Continue on reverse side if necessary and identify by block number) Phase-Locked Loop Frequency Synthesizer		

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The results of the design and fabrication of a phase-locked loop frequency synthesizer suitable for local oscillator function in a receiver is presented. The

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S/N 0102-014-6601

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(20. ABSTRACT Continued)

electronically tunable synthesizer operates in the frequency band from 47.5 MHz to 97.5 MHz in steps of 25 kHz and is accurate to within ±0.0018% of the programmed frequency.

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An Electronically Tunable Frequency Synthesizer Design For An UHF Receiver

by

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Lieutenant, Turkish Navy
B.S.E.E., Naval Postgraduate School, 1979

Submitted in partial fulfillment of the
requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

from the

NAVAL POSTGRADUATE SCHOOL
December 1979

ABSTRACT

The results of the design and fabrication of a Phase-Locked Loop frequency synthesizer suitable for local oscillator function in a receiver is presented. The electronically tunable synthesizer operates in the frequency synthesizer operates in the frequency band from 47.5 MHz to 97.5 MHz in steps of 25 kHz and is accurate to within ±0.0018% of the programmed frequency.

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LIST OF SYMBOLS AND ABBREVIATIONS

BCD	Binary coded decimal
ECL	Emitter coupled logic
EPROM	Erasable read only memory
IC	Integrated circuit
IF	Intermediate frequency
PLL	Phase-locked loop
PROM	Programmable read only memory
TTL	Transistor transistor logic
VCO	Voltage-controlled oscillator
VVC	Voltage variable capacitor
f_{out}	Output frequency
f_{ref}	Reference input frequency
$\theta_e(s)$	Error phase
$\theta_i(s)$	Input phase
$\theta_o(s)$	Output phase
K_f	Filter/amplifier gain
k_n	Integer devisor
K_v	Voltage-controlled oscillator gain
δ	Damping ratio
ω_n	Natural frequency

ACKNOWLEDGEMENT

The author would like to express his sincere thanks and appreciation to Professor Donald A. Stentz for his advice and assistance.

I. INTRODUCTION

As a general concept, all devices generating output frequencies which are rational multiples of a standard input frequency are known as frequency synthesizers. The synthesizer of interest in this thesis can generate one frequency out of a large number of output frequencies on external command. Probably the greatest impetus to frequency synthesizer development has been the demand for communication capability within a limited spectrum. By providing accurate frequency control at reasonable costs, frequency synthesizers provide a maximum number of channels for an available total bandwidth. Perhaps equally important, this frequency control can be obtained by relatively untrained operators.

Before the solid state age of electronics, frequency synthesizer techniques generally consisted of analog circuit technology utilizing variable tuned LC circuits, and vacuum tube components. Such systems were not synthesizers, although they were commonly described as such. They have also been referred to by other names, such as stabilized master oscillators. The frequency stability of these oscillators was not adequate for many applications such as communications systems, where rapid, accurate frequency acquisition was necessary. Frequency stability can be improved by using a

crystal oscillator, but the range of frequencies available from one oscillator is limited to a small band about the resonant frequency of the cyrstal or to harmonics of the crystal frequency. The divide-by-N, phase-lock synthesizer became practical with the advent of the high-speed digital integrated circuit. The application of phase-lock loops involving active elements has the advantage of simpler and cheaper selective circuits. The basic technique used with integrated circuits is one of a digital phaselock closed loop. Inserted within the feedback loop is a programmable digital divider to provide the multi-channel capability required for communications. This system provides that with only one crystal reference source all the channel requirements can be generated to accommodate its use for a communication transmitter or receiver.

The design presented in this thesis describes a phase-lock loop frequency synthesizer suitable for the local oscillator in the UFH receiver. The required frequency range of the UHF equipment for transmitter operation is 200 MHz to 400 MHz. The synthesizer in this thesis is intended for frequency conversion to an IF frequency of 10 MHz. The required frequency range of the synthesizer is then 190 MHz to 390 MHz.

The required channel spacing between two frequencies is 0.1 MHz. The synthesizer was implemented with standard integrated circuits. Discrete transistors are used as

translators and amplifiers for convenience and improved loop performance. An erasable read only memory (EPROM) is used for frequency conversion to an IF frequency.

The synthesizer was planned consisting of two basic blocks. The first block is a phase-lock loop which operates within the frequency band of 47.5 MHz to 97.5 MHz with 25 kHz channel spacing and gives 2.5 MHz frequency conversion of the IF frequency. The second block is a multiplication by a factor of 4 circuit which would give the required frequency band of 190 MHz to 390 MHz with 100 KHz channel spacing and 10 MHz IF frequency. In this thesis, only the first phase-lock loop block was designed and implemented.

II. SYNTHESIZER DESIGN PHILOSOPHIES AND DEFINITIONS

A. FREQUENCY SYNTHESIS

A frequency synthesizer is a combination of system elements that results in the generation of one or many frequencies from one or a few reference sources. In its early form, it was a crystal-controlled oscillator with a bank of crystals switched in manually. The frequency accuracy and stability of this device were determined by the accuracy and stability of the crystal and, to a lesser extent, the circuit. The crystal-controlled oscillator was superseded, but not replaced, by an approach presently known as incoherent synthesis. This technique utilizes a number of crystal-controlled oscillators combined in such a fashion as to generate many frequencies with relatively few crystals.

While these improvements took place, the rapidly growing field of communications developed requirements for more sophisticated frequency generation systems demanding accuracies and stabilities higher by orders of magnitude than incoherent synthesis could provide. To meet the requirements, a new family of approaches grouped under the name of coherent synthesis, emerged. As the name implies, these approaches provide means for producing many frequencies from one reference source having the required accuarcy and stability. These techniques resulted in the generation of

spurious outputs, which had to be eliminated by a proper choice of frequencies used in the synthesis and suppressed by filtering.

1. Incoherent Synthesis

The manner in which output frequencies are generated from input frequencies in incoherent synthesis varies depending on the application, output frequency range, value of the smallest frequency increment, frequency stability and accuracy, levels of spurious outputs, size, cost, and power consumption. These are the factors governing the choice of an approach. The principal goal of this technique is to minimize the number of crystals and basic building blocks such as oscillators, mixers, and filters used in synthesis in order to achieve the optimum characteristics and cost.

2. Coherent Direct Synthesis

The principal difference between incoherent and coherent synthesis is the number of frequency sources utilized in the process of frequency generation. In the first approach there are numerous crystal-controlled oscillators; in the second only one reference source is used. Hence the stability and accuracy of the output frequency in a coherent direct synthesis system are the same as the stability and accuracy of the reference source.

3. Coherent Indirect Synthesis

Indirect synthesis utilizes the princple of feedback in generating frequency increments. The technique, known as phase locking, differs from direct synthesis in many

respects. The system analysis of indirect synthesis centers on an investigation of phase-locked loop stability and acquisition, not on spurious outputs. Voltage-controlled oscillators, programmable dividers, phase detectors, and frequency discriminators are two building blocks used.

B. SYNTHESIZER PROPERTIES

The frequency synthesizer is a relatively complicated system involving many components. Usually a number of properties must be specified in order to characterize performance. However there is no uniform standard to describe or measure many of these parameters.

1. Frequency Standard

The reference frequency (f_{ref}) can be chosen for convenience of oscillator and crystal design. Low cost crystal oscillators can be purchased with a long-term aging rate of about one part in 10^6 parts per year.

2. Resolution

Resolution is the minimum frequency difference between any two adjacent output frequencies. Synthesizers usually generate all frequencies within a specified output band with identical spacing. Resolution large depends on the application.

3. Number of Frequencies

Synthesizers may be able to generate an output on any one of as few as 100 discrete output frequencies, although some synthesizers can generate any one of 5×10^9

discrete output frequencies. The number of discrete frequencies generated largely depends on its ultimate use.

4. Programmability

The output frequencies of essentially all modern frequency synthesizers are specified by the DC levels on a set of control wires. The advantages of this approach are:

a. Remote Control.

b. Optimum layout to minimize spurious radiations, even when frequency control is derived from the front panel.

c. More rapid and reliable control than with mechanical systems.

5. Switching Time

The switching time is the elapsed time between a command to switch to a different frequency and the time when the output is available. Typical worst-case switching speeds range from 1 msec to about 10 μsec, and synthesizers with switching speeds less than 1 μsec have been demonstrated.

III. UNDERSTANDING BASIC PLL SYNTHESIZER

The majority of all phase-locked loop synthesizers consist of a phase detector, filter, voltage-controlled oscillator (VCO) and a programmable counter as shown in Figure 1.

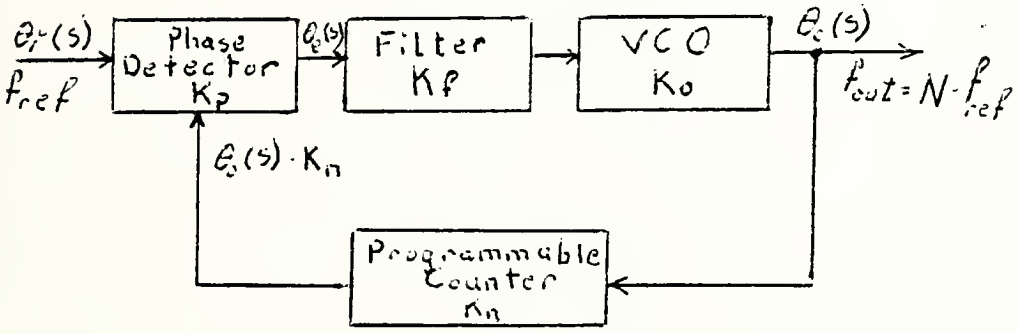


Figure 1. PHASE-LOCKED LOOP SYNTHESIZER

The symbols in Figure 1 can be explained as follows:

f_{ref} = reference input frequency

$\theta_i(s)$ = input phase

$\theta_e(s)$ = error phase

$\theta_o(s)$ = output phase

f_{out} = output frequency

K_p = phase detector gain (volt/radian)

K_f = amplifier/filter gain

K_v = VCO gain (rad/sec/volt)

K_n = Integer divisor ($K_n = 1/N$)

K_o = Kv/s (rad/sec/volt)

The s in the denominator converts the frequency characteristics of the VCO to phase.

The phase detector produces a voltage proportional to the phase difference between the signals θ_i and θ_o/N. This voltage upon filtering is used as the control signal for the voltage controlled oscillator (VCO). Since the VCO produces a frequency proportional to its input voltage, any time variant signal appearing on the control signal will frequency modulate the VCO. The output frequency is $f_o = Nf_i$ during phase lock. The phase detector, filter, and VCO, compose the feed forward path with the feedback path containing the programmable divider. Various types and orders of loops can be constructed depending upon the configuration of the overall loop transfer function.

IV. EXPERIMENTAL PROCEDURE AND SYSTEM DESIGN

In this thesis, the required frequency range is 190 MHz to 390 MHz. However, available oscillators on the market cannot meet this required wide frequency range. To implement the design first a PLL was built within the frequency range 47.5 MHz to 97.5 MHz which provides a 2.5 MHz IF. The required channel spacing was 25 kHz which required a 2.5 KHz reference frequency. To produce a reference frequency of 25 kHz a 1 MHz signal from a frequency standard was used and it was divided by a factor of 10 first and then by a factor of 4. The output of the PLL was intended to be multiplied by a factor of 4. After multiplication the output frequency range meets the required frequency band and provides an IF frequency of 10 MHz with channel spacing of 100 kHz. This multiplication operation can be achieved simply by using two cascaded frequency doublers. A simplified block diagram of the synthesizer is shown in Figure 2.

A. BINARY CODED DECIMAL (BCD) SWITCHES

Four BCD switches are used to achieve the external command control. The external command is a decimal number determined by the position of the thumbwheel switches which in turn are set to indicate the desired frequency.

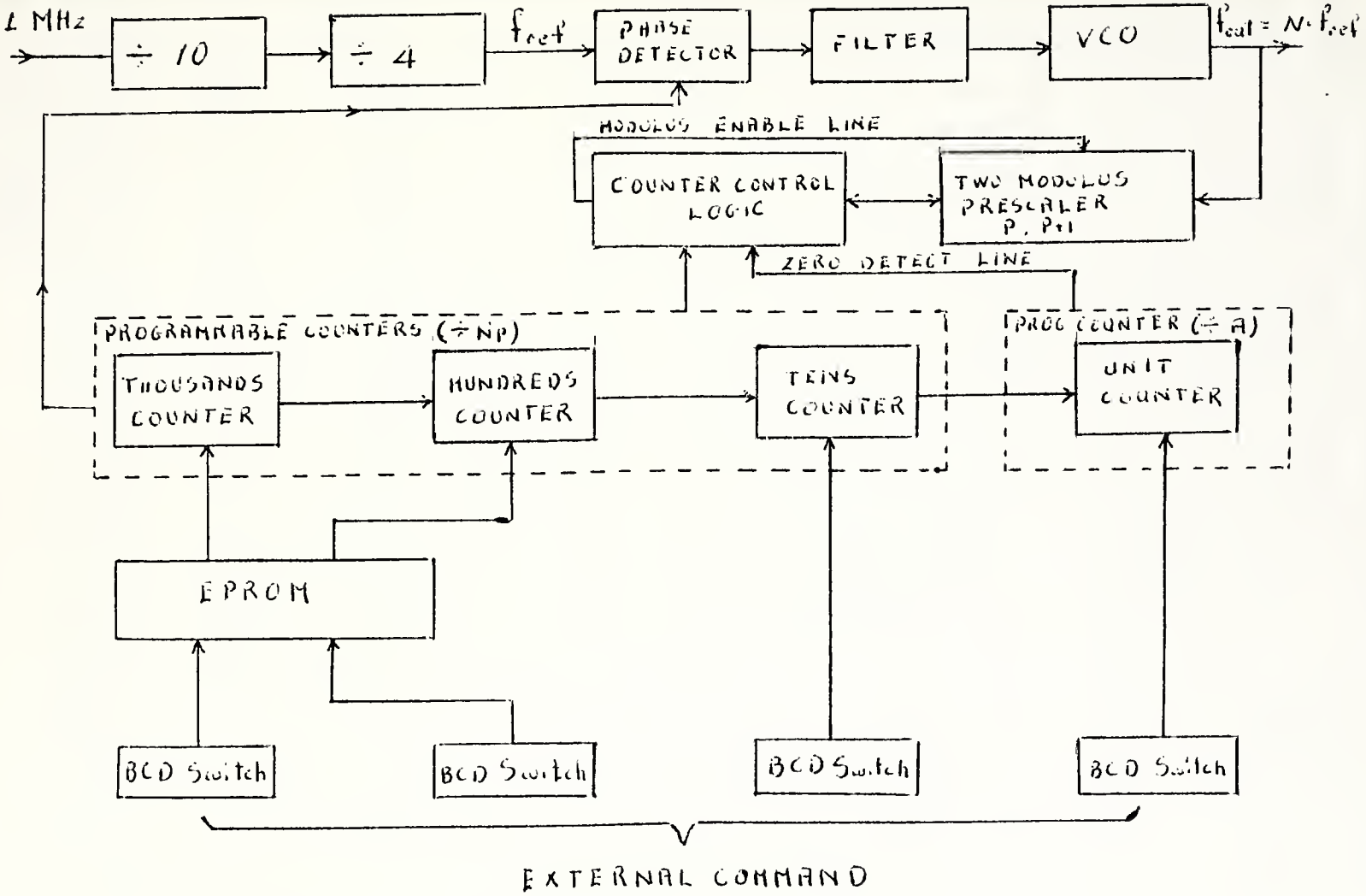


Figure 2. SIMPLIFIED BLOCK DIAGRAM OF SYNTHESIZER

If an operator wants an output frequency of 251.1 MHz, he simply sets the first BCD switch to 2, and second to 5, third to 1, and fourth to 1. The output of these switches is the binary equivalent of the decimal number on the thumbwheels. Standard 1-2-4-8 weighting is used. Cascaded counters are driven directly by these outputs.

B. PROGRAMMABLE READ ONLY MEMORY

To produce the required IF frequency of 2.5 MHz at the output of the PLL, the programmable counter had to count 100 less than the actual external command. For transmitter operation, when the operator sets the thumbwheel switches to N = 2000, the output frequency is N times the reference frequency. Since a reference frequency of 25 kHz was used,

$$f_{out} = N \times f_{in} = 2000(25 \times 10^3 \text{ Hz})$$

$$= 50 \text{ MHz}$$

the operator sets the thumbwheel switches with the same number

$$f_{out} = 1900(25 \times 10^3 \text{ Hz}) = 47.5 \text{ MHz}.$$

To meet this requirement, an external command on the thumbwheel switches was decoded by using a programmable read only memory (PROM).

An 8K UV Erasable PROM CS2708 was used for this purpose. One advantage of using an EPROM was the simplicity of IF conversion. One can change the IF frequency simply by changing the decoding logic stored in the EPROM. Since only 100 less counts are required, this is achieved by only decoding the first two digits of the external command. The data at the outputs of the first two binary coded decimal (BCD) switches are connected to the address lines of EPROM, and the decoded outputs are used to drive the first two decade counters circuit as shown in Figure 3.

C. VOLTAGE CONTROLLED OSCILLATOR

The MC1648 emitter-coupled oscillator, constructed on a single monolithic chip, is used to implement the design. Output levels are emitter coupled logic levels (ECL). The oscillator requires an external parallel tank circuit consisting of the inductor (L) and capacitor (C). The MC1404, an epicap hyper-abrupt junction tuning diode is incorporated into the tank circuit to provide a voltage variable input for the oscillator. Epicaps are voltage variable capacitors based on PN junction theory. The capacitance value of the device actually varies as a function of applied voltage, and this specific mechanism permits the device to function as an epicap, or voltage variable capacitor (VVC). Details on the theoretical considerations are explained in Reference 3. Figure 4. is taken from Reference. 3.

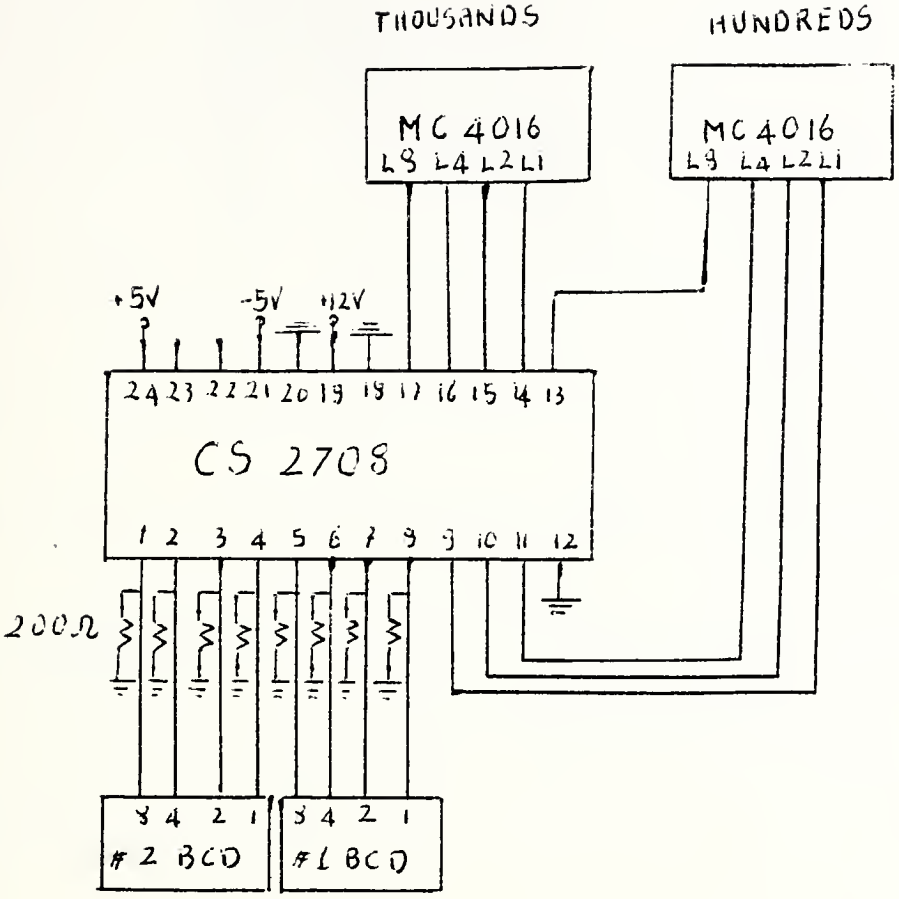


Figure 3. CS2708 EPROM

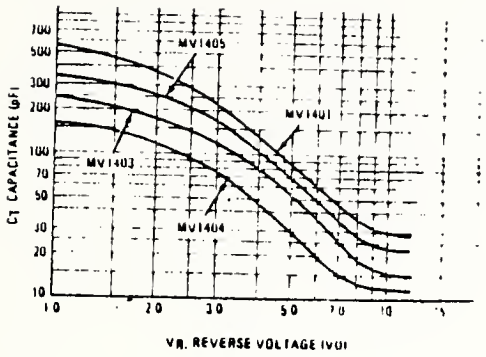


Figure 4. DIODE CAPACITANCE VERSUS REVERSE VOLTAGE

The capacitance value of the MV1404 diode changes between 15 pF and 200 pF. Input capacitance of the MC1648 is typically 6 pF. The tuning range of the oscillator is calculated as follows:

$$f = \frac{1}{2\pi \sqrt{LC}}$$

where: $C = C_{diode} + C_{input}$.

$$f_{min} = \frac{1}{2\pi \sqrt{L\ C_{max}}}$$

$$f_{max} = \frac{1}{2\pi \sqrt{L\ C_{min}}}$$

The required values for f_{min} and f_{max} are respectively 47.5 MHz and 97.5 MHz. Minimum and Maximum capacitance values are taken from the graph in Figure 4.

By using the equations given above, the inductance value (L) is found to be approximately 0.11 μH. A micro-metal toroidal core with 3 turns of No. 20 copper wire around it is used as an inductor in the tank circuit. Configuration of this oscillator is shown in Figure 5.

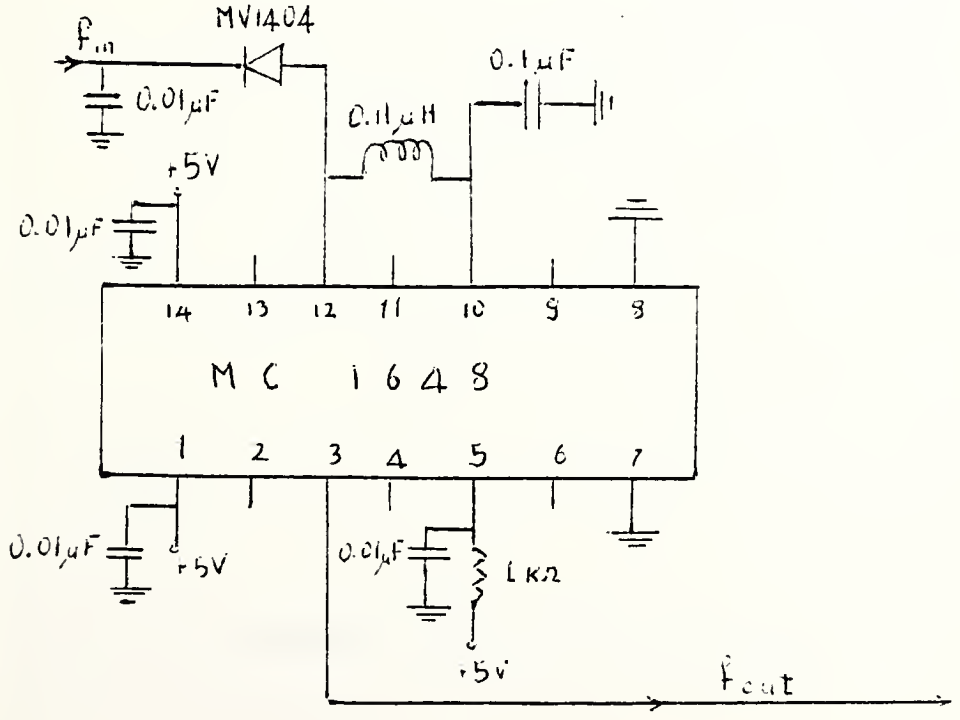


Figure 5. VOLTAGE CONTROLLED OSCILLATOR

The transfer characteristics of this oscillator is shown in Figure 6.

The oscillator gain constant was found to be

$$K_V = 87,166 \times 10^6 \text{ rad/sec/volt}$$

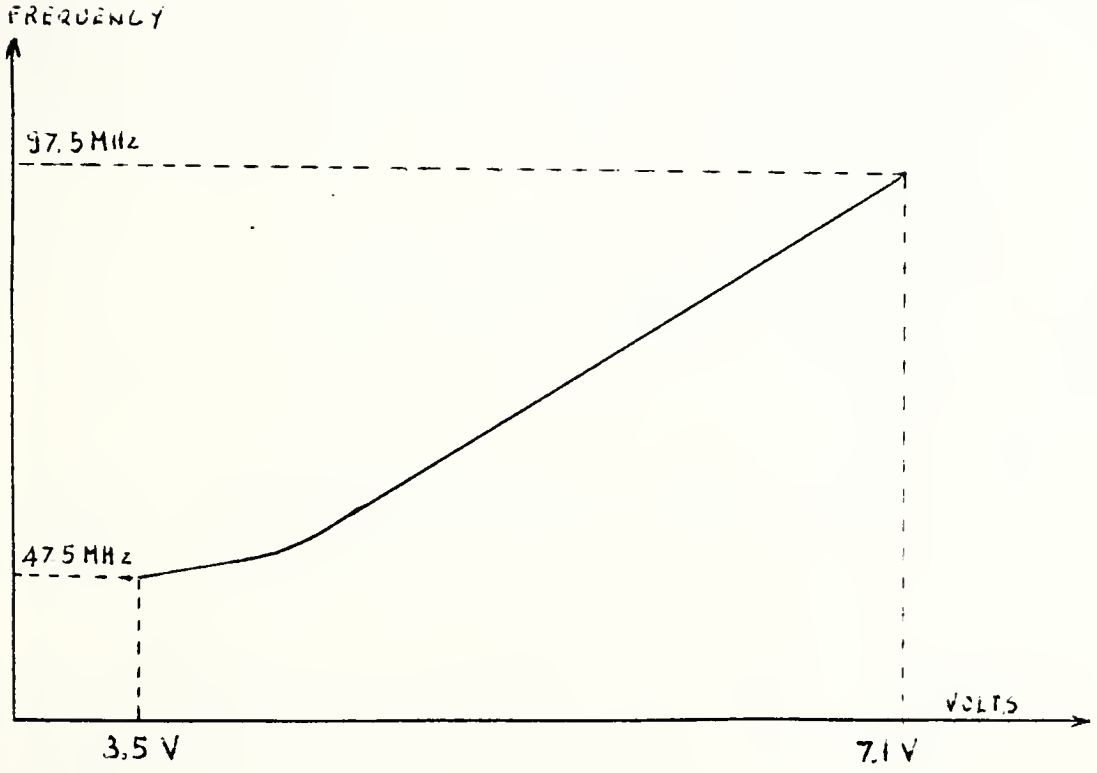


Figure 6. TRANSFER CHARACTERISTICS OF THE VCO

D.. VARIABLE MODULUS RESCALER

Emitter-coupled logic levels at the output of the VCO were not high enough to drive the programmable counters, and the highest frequency that the counters can operate at is 8 MHz. Just a few years ago, to overcome these problems, fixed prescalers began to be used in phase-locked loops, as shown in Figure 7.

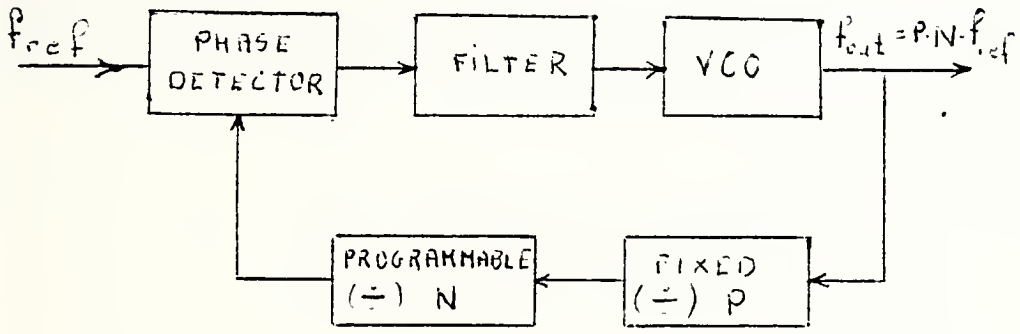


Figure 7. FREQUENCY SYNTHESIS BY USING ONE FIXED PRESCALER

P is fixed and N is variable. For a change of 1 in N, the output frequency changes by $P \cdot f_{ref}$. If f_{ref} equals the desired channel spacing, then, only every P channel may be programmed using this method. The disadvantage of using a fixed modulus, (% P), for frequency division in high frequency phase-locked loops is that it requires dividing

the desired reference frequency by P also. Such a system is shown in Figure 8.

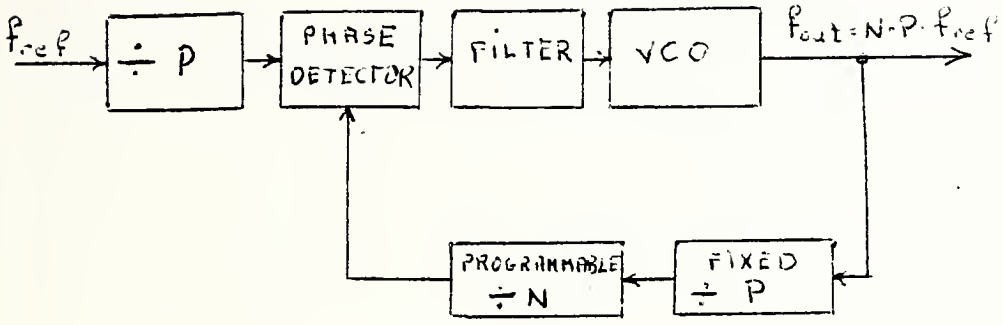


Figure 8. FREQUENCY SYNTHESIS BY USING TWO FIXED PRESCALERS

A (%P) is placed in series with the desired channel spacing to give a reference frequency. A problem still remains because the design of an optimum loop filter requires that the input reference frequency be as high as possible where the upper limit is established by the required channel spacing. Another solution is found by using the technique

known as variable modulus prescaling. The use of this technique permits direct high frequency prescaling without any sacrifice in resolution since it is no longer necessary to divide the reference frequency by the modulus of the high frequency scaler.

The theory of variable modulus prescaling is explained by considering the equation for f_{out}. From Figure 7,

$$f_{out} = N \cdot P \cdot f_{ref} \qquad (1)$$

From this equation it may be seen that only every P channel can be programmed simply, because N is always an integer. To obtain intermediate channels, P must be multiplied by an integer plus a fraction. The fraction would be of the form A/P. If N is defined to be an integer number, Np, plus a fraction A/P, N may be expressed as:

$$N = Np + A/P$$

Substituting this expression for N in the output equation gives:

$$f_{out} = (Np + A/P) \cdot P \cdot f_{ref} \qquad (2)$$

or

$$f_{out} = (N_p \cdot P + A) \cdot f_{ref} \qquad (3)$$

$$f_{out} = N_p \cdot P \cdot f_{ref} + A \cdot f_{ref} \qquad (4)$$

Equation (4) shows that all channels can be obtained directly if N can take on fractional values. Since it is difficult to multiply by a fractional number, taking equation (3) and adding $\pm AP$ to the coefficient of f_{ref}, the equation becomes:

$$f_{out} = (N_p \cdot P + A + A \cdot P - A \cdot P) \cdot f_{ref} \qquad (5)$$

Collecting terms and factoring gives:

$$f_{out} = [(N_p - A)P + A(P+1)] \cdot f_{ref} \qquad (6)$$

From equation (6) it becomes apparent that the fractional part of N can be synthesized by using a two modulus counter (P and P+1) and dividing the upper modulus by A and the lower modulus by $(N_p - A)$. Equation (6) suggests the circuit configuration of Figure 9. The MC12012 variable two modulus prescaler is used in this design. The MC12012 consists of three functional blocks:

1. A controllable divide by 5 divide by 6 prescaler.
2. A divide by 2 prescaler.
3. Conversion of ECL to transistor transistor logic (TTL).

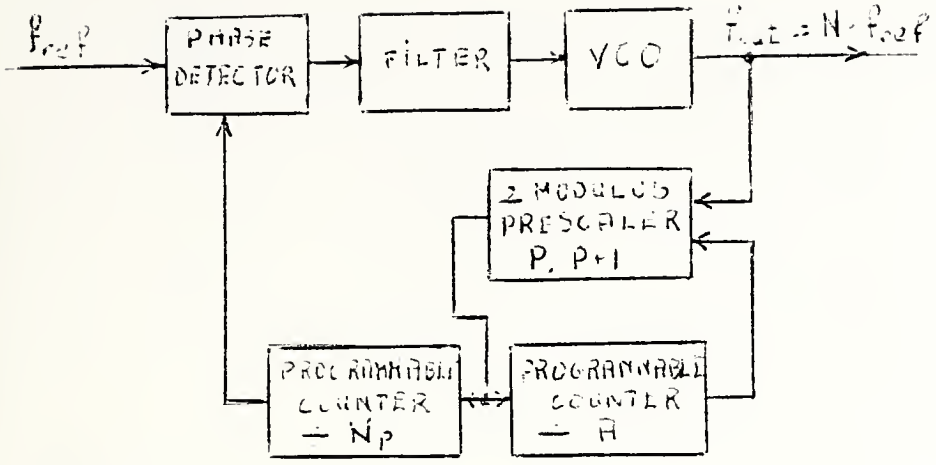


Figure 9. FREQUENCY SYNTHESIS BY TWO VARIABLE MODULUS PRESCALING

The ÷5/÷6 prescaler is connected externally to the ÷2 prescaler to form a ÷10/÷11 prescaler. This configuration is shown in Figure 10. The technique and system described in this thesis is a new approach to the construction of a phase-locked loop divider. In addition to using the MC12012 variable modulus prescaler, this system requires an MC12014 counter-control-logic-function, together with suitable counters.

E. COUNTER CONTROL LOGIC

The MC12014 monolithic counter control logic is used in this design. The MC12014 is designed for use with the MC12012 two-modulus prescaler and the MC4016 programmable

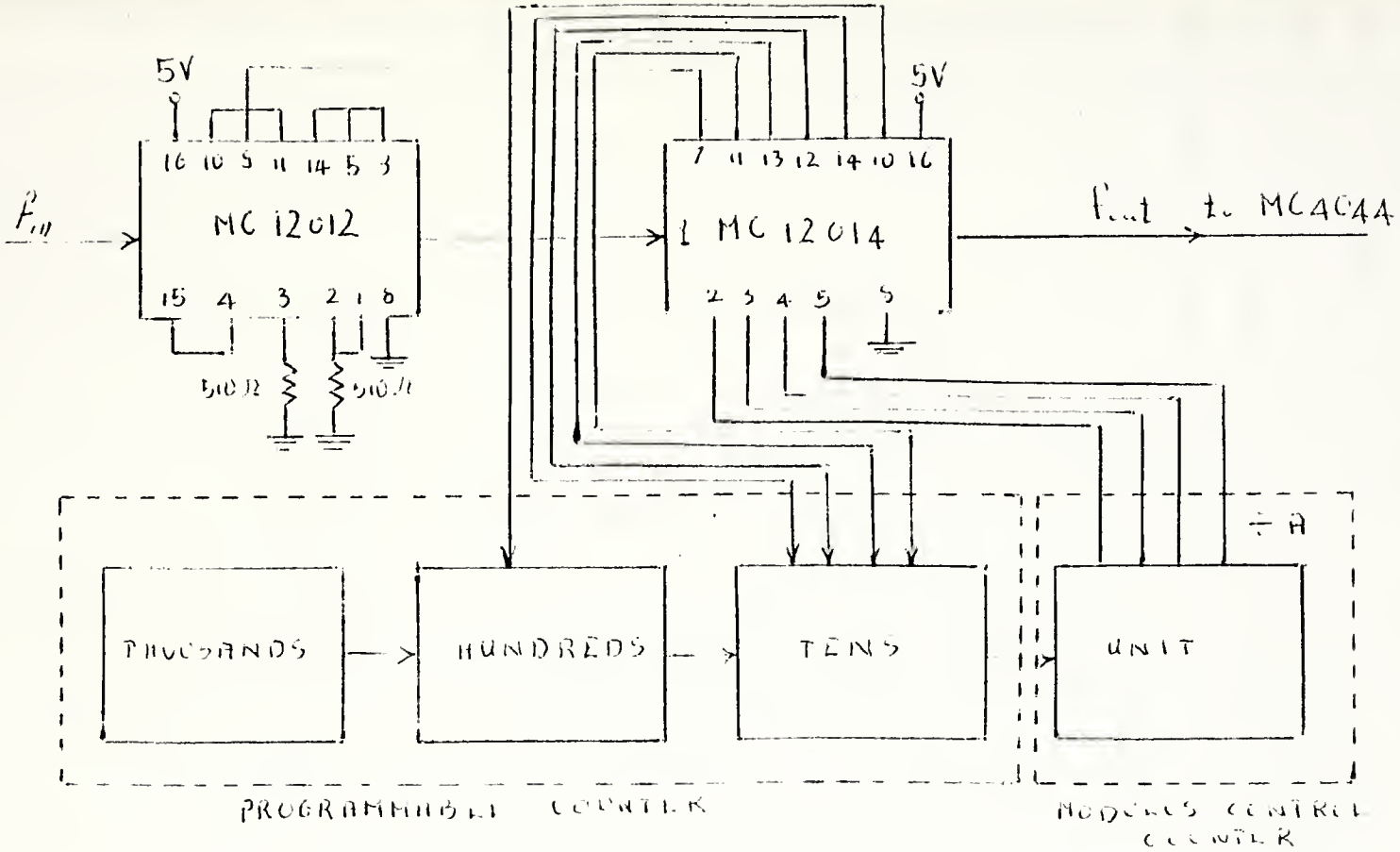


Figure 10. FREQUENCY DIVISION

counter to accomplish direct high frequency programming. The MC12014 consists of a zero detector which controls the modulus of MC12012, and an early decode function which controls the programmable counters. The early decode feature also increases the useful frequency range of the programmable counter from 8.0 MHz to 25 MHz. The operation of the MC12014 with the MC12012 is best explained by considering Figure 10. The MC12012 dual modulus prescaler divides by either 10 or 11 when connected as shown in Figure 10. If the enable line is high at the start of the prescaler scycle, division by 10 results, if the enable input is low at the beginning of the cycle, division by 11 results. The zero detection circuitry of the MC12014 counter control logic was connected to monitor the outputs of the modulus control counter; this provided a suitable enable signal at pin 7 as the modulus control counter reached its terminal (zero) count. The remainder of the MC12014 is connected to extend the operating frequency of the programmable counter chain.

F. ANALYSIS OF THE PROGRAMMABLE COUNTER

Counters may normally be connected together in sequence, so the output of the first is the input to the second, and so on to lengthen the count. In this case, the resulting divisor N will be the product of the modulus of the two counters. Normally, ripple counters clock on the falling or negative edge of the clock, so that as the output of one

counter drops, it triggers the next down the line. With some synchronous counters, the advance of the counter on the positive-going clock edge and logic from a previous group of stages enables the input to a following stage so it advances in synchronism with the clock edge. Unit decade cascadable counters are another possibility. For many long programmable count sequences, it would be desirable to have a series of thumbwheel switches. If one dials a 425 into these switches it is desired that the counter divide by four hundred twenty five. If one simply connects three ordinary divide-by-n counters so one output drives the next input, we would divide by $4 \times 2 \times 5$, or 40, instead, and the situation would get very confusing if one of the counters should happen to be set at 0. What is needed is a counting system that allows 400 counts plus 20 counts plus 5 counts to get the total desired. Ordinary counters will not do this, and it takes a combination of look-ahead and feedback techniques to handle this problem. The 4016 and 4018 series counters are unit cascadable and work on a down-count basis. Each successive stage detects count 0, and an output pulse 0 is then produced only if all the stages are simultaneously 0. This detected 0 is then used to reload the number to be divided back into the counter for the next round. In this design, four MC4016 unit decade cascadable counters are used to implement the programmable counter chain. Configurations are shown in Figure 11.

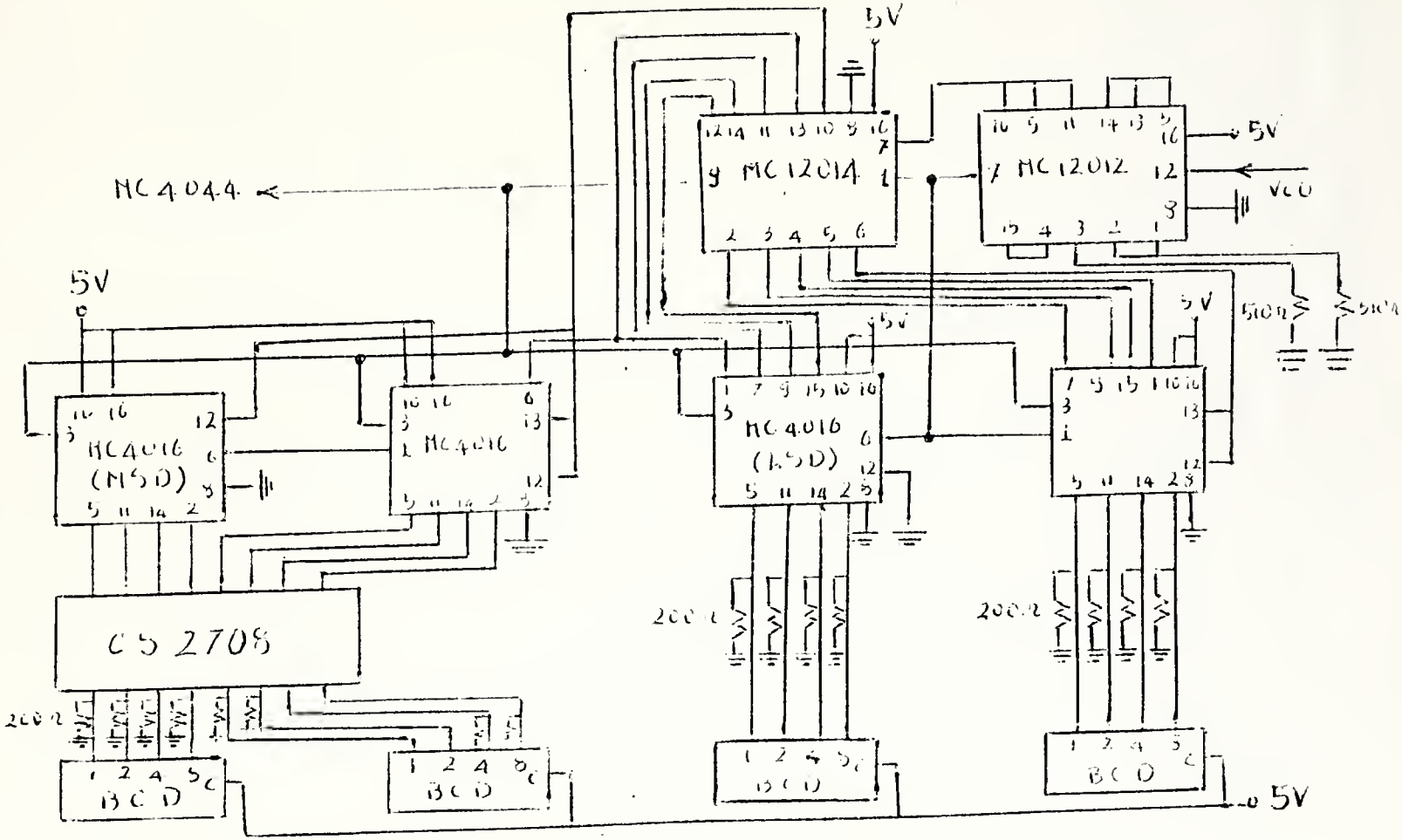


Figure 11. PROGRAMMABLE COUNTER

G. DIVIDE BY 10 AND DIVIDE BY 4 CIRCUITS

To generate the 25 kHz reference frequency a 1 MHz standard frequency source is used. First it is divided by a factor of 10. This is accomplished by using the decade counter 74LS90. The circuit is shown in Figure 12.

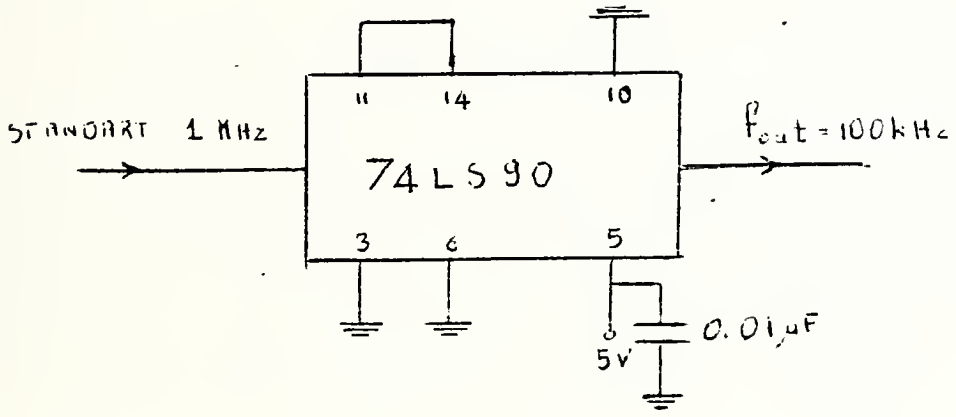


Figure 12. DIVIDE BY 10 CIRCUIT

The 100 kHz output frequency of the decade counter is fed to the binary counter 74LS93 to divide by a factor of 4. This circuit is shown in Figure 13.

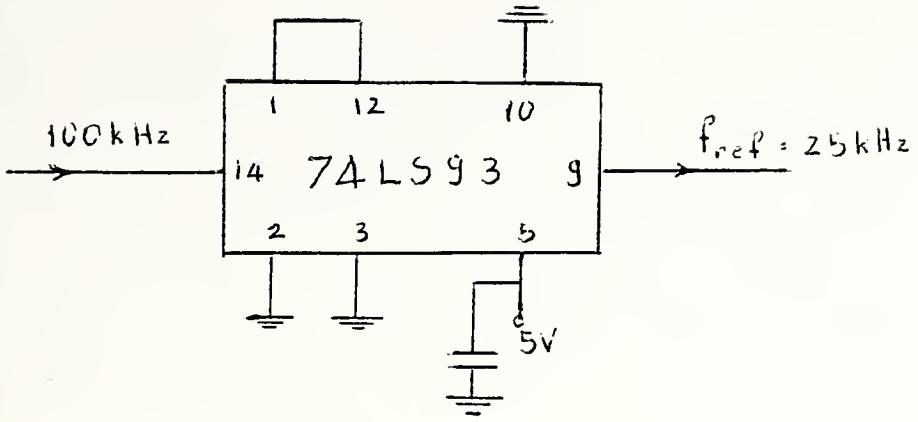


Figure 13. DIVIDE BY 4 CIRCUIT

H. PHASE DETECTOR, LOOP FILTER AND PLL DESIGN

The MC4044 phase-frequency detector is used as the phase detector. It consists of two digital phase detectors, a charge pump, and an amplifier as shown in Figure 14.

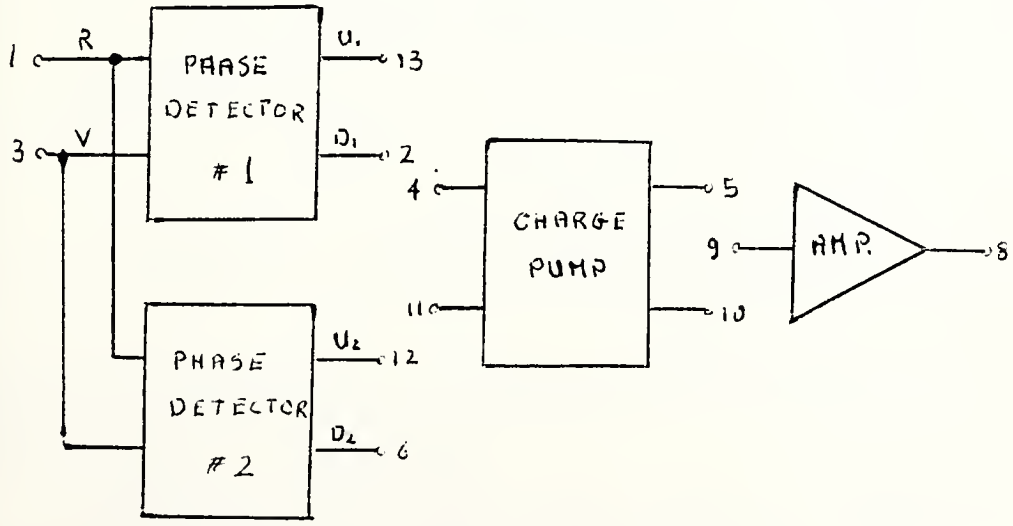


Figure 14. MC4044 PHASE DETECTOR

The circuit accepts TTL waveforms at the R and V inputs and generates an error voltage that is proportional to the frequency and/or phase difference of the input signals. Phase detector #1 is intended for use in systems requiring zero frequency and phase difference at lock. Phase detector #2 is used if quadrature lock is desired. Phase detector #1 and the charge pump section are connected as shwon in Figure 15.

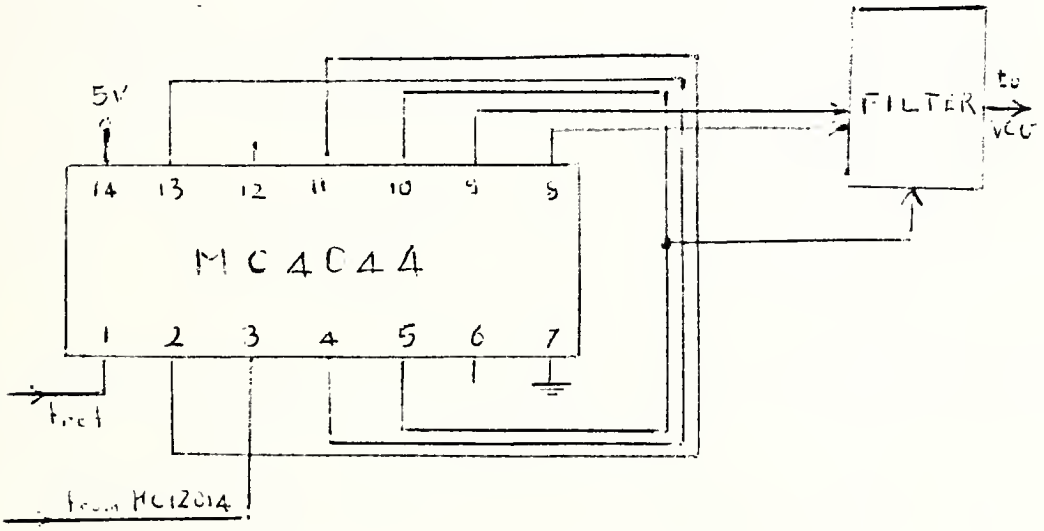


Figure 15. THE MC4044 PHASE DETECTOR

The phase detector gain constant for the MC4044 phase detector is K_p = 0.111 V/rad.

A fundamental phase-locked loop frequency synthesizer consists of a phase detector, amplifier/filter,

voltage-controlled oscillator and a programmable divide-by-N circuit in the feedback loop. Fundamental loop characteristics such as capture range, loop bandwidth, capture time and transient response are controlled primarily by the loop filter. In this design the parameters determined included K_p, K_o and K_n leaving only K_f as the variable for the design.

The output to input ratio reflects a second order low-pass filter frequency response.

$$\frac{\theta_o(s)}{\theta_i(s)} = \frac{K_p K_f K_v}{S + K_p K_f K_v K_n} \qquad (1)$$

where $$K_f = \frac{1 + T_1 S}{T_2 S} \qquad (2)$$

More details on theoretical considerations are explained in References 1 and 2.

The Laplace representation of the design is shown in Figure 16. The operational amplifier in the MC4044 is used to accomplish the active filter design. This circuit is shown in Figure 17.

K_f is expressed by

$$K_f = \frac{R_c CS + 1}{R_1 CS} \qquad (3)$$

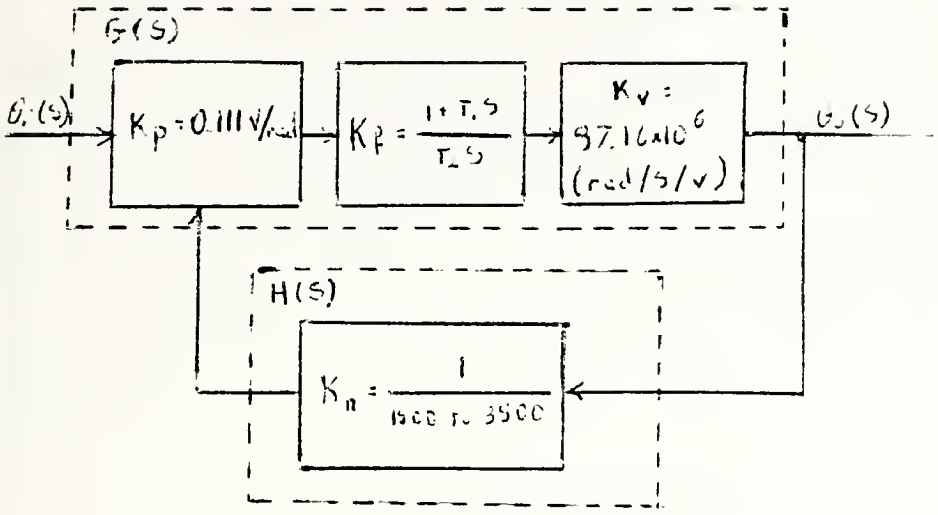


Figure 16. LAPLACE REPRESENTATION OF THE DESIGN

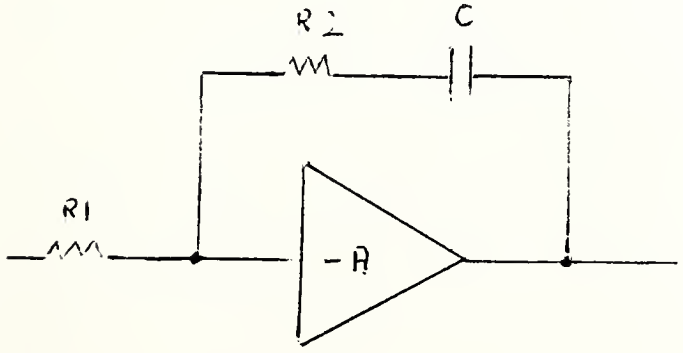


Figure 17. ACTIVE FILTER DESIGN

for large A, where A is the voltage gain of the amplifier. R_1, R_2 and C are then the variables used to establish the overall loop characteristics. As stated in Reference 4, since the gain of the active filter circuitry in the MC4044 is not infinite, a gain correction factor, K_c, has to be applied to K_f in order to properly characterize the function. K_c is found experimentally to be $K_c = 0.5$. As stated in Reference 2,

$$K_{f_c} = K_f \cdot K_c = 0.5\left(\frac{R_c CS + 1}{R_1 CS}\right) \qquad (4)$$

The loop transfer function for the circuit diagram in Figure 17 is

$$G(S)H(S) = K_p K_{f_c} K_o K_n \cdot$$

$$G(S)(H(S) = K_p(0.5)\left(\frac{R_2 CS + 1}{R_1 CS}\right)\left(\frac{K_v}{S}\right)\left(\frac{1}{N}\right) \qquad (5)$$

The characteristic equation, (CE), took the form

$$CE = 1 + G(S)H(S) = 0 \qquad (6)$$

$$CE = S^2 + \frac{0.5K_p K_v R_2}{R_1 N} S + \frac{0.5K_p K_v}{R_1 CN} \qquad (7)$$

Relating this equation to the standard form of CE

$$CE = S^2 + 2\delta\omega_n S + \omega_n^2 \tag{8}$$

and equating the coefficients yields

$$\omega_n^2 = \frac{0.5K_pK_v}{R_1CN} \tag{9}$$

and

$$2\delta\omega_n = \frac{0.5K_pK_vR_2}{R_1N} \tag{10}$$

where ω_n is the natural frequency and (δ) is the damping ratio. The percent overshoot and settling time are used to determine the natural frequency ω_n.

A damping ratio (δ) of 0.60 is chosen to produce a peak overshoot less than 25%. This is shown in Figure 18 which was taken from Reference 8.

The steady state frequency of the system is assumed to be 5% of the normalized output frequency. This gives $\omega_n t = 5.96$. The required lock up time is assumed to be 4.5 msec. The natural frequency is found to be

$$\omega_o = 1324 \text{ rad/sec.}$$

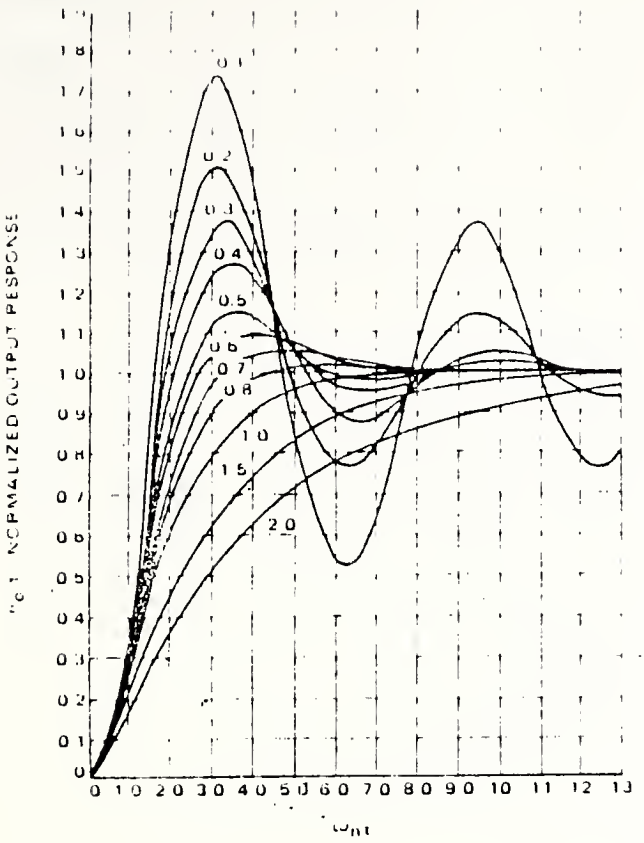


Figure 18. TYPE 2 SECOND ORDER STEP RESPONSE

Rewriting equation (9) gives

$$R_1C = \frac{0.5K_pK_v}{\omega_n^2 N}$$

Maximum overshoot occurs at N_{max} which occurs at minimum loop gain. The determined loop parameters are found to be

$$K_p = 0.111 \text{ Volt/rad}$$

$$K_v = 87{,}166 \times 10^6 \text{ R/sec/V}$$

ω_n = 1324 Hz

N_{max} = 3900

R_1C is found to be 0.7076×10^{-3},

C is chosen as 0.47 μF, and

R_1 is found to be 1.5 Kohms.

From equation (10) R_2 is found to be 1.5 Kohms. All circuit circuit parameters have been determined and the PLL properly configured. The schematic for the loop filter is shown in Figure 19.

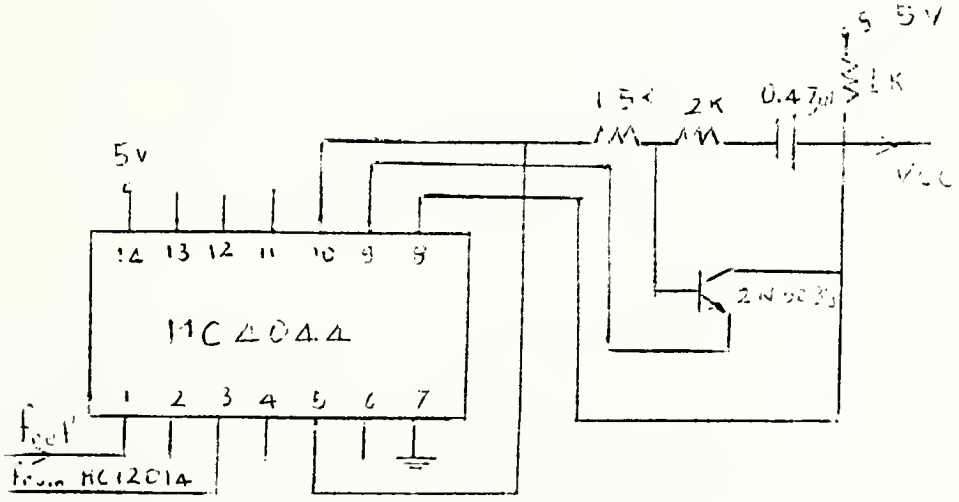


Figure 19. LOOP FILTER

An available resistor of 2 Kohms was used to build the circuit instead of 1.9 Kohms, with no apparent degradation of circuit characteristics. The output of the VCO was observed and it was noted that an additional active filter was needed to reduce the 25 kHz reference frequency appearing at the output. This filter is diagrammed in Figure 20.

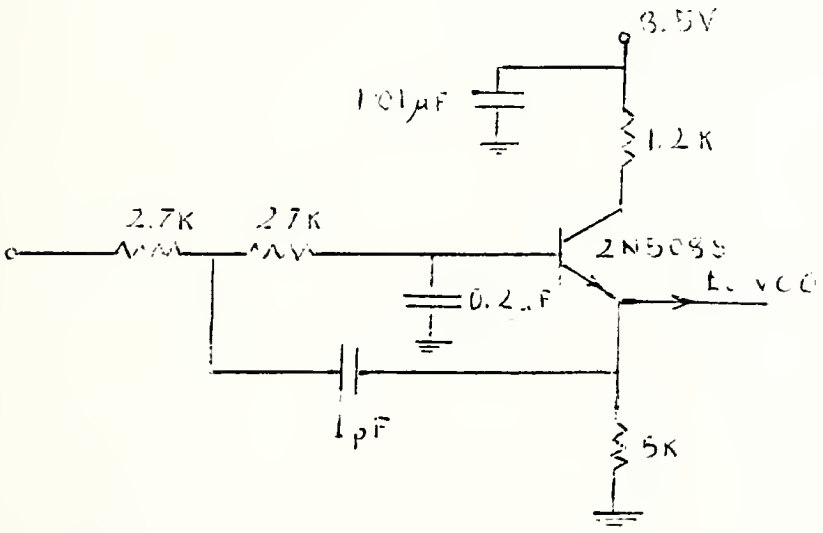


Figure 20. ADDITIONAL ACTIVE FILTER

To insure reasonable isolation with the phase-lock loop, the corner frequency of this active filter was set expermentally by changing the capacitor values. Details about

this filter are found in Reference 4. The complete shcematic of the synthesizer is shown in Figure 21.

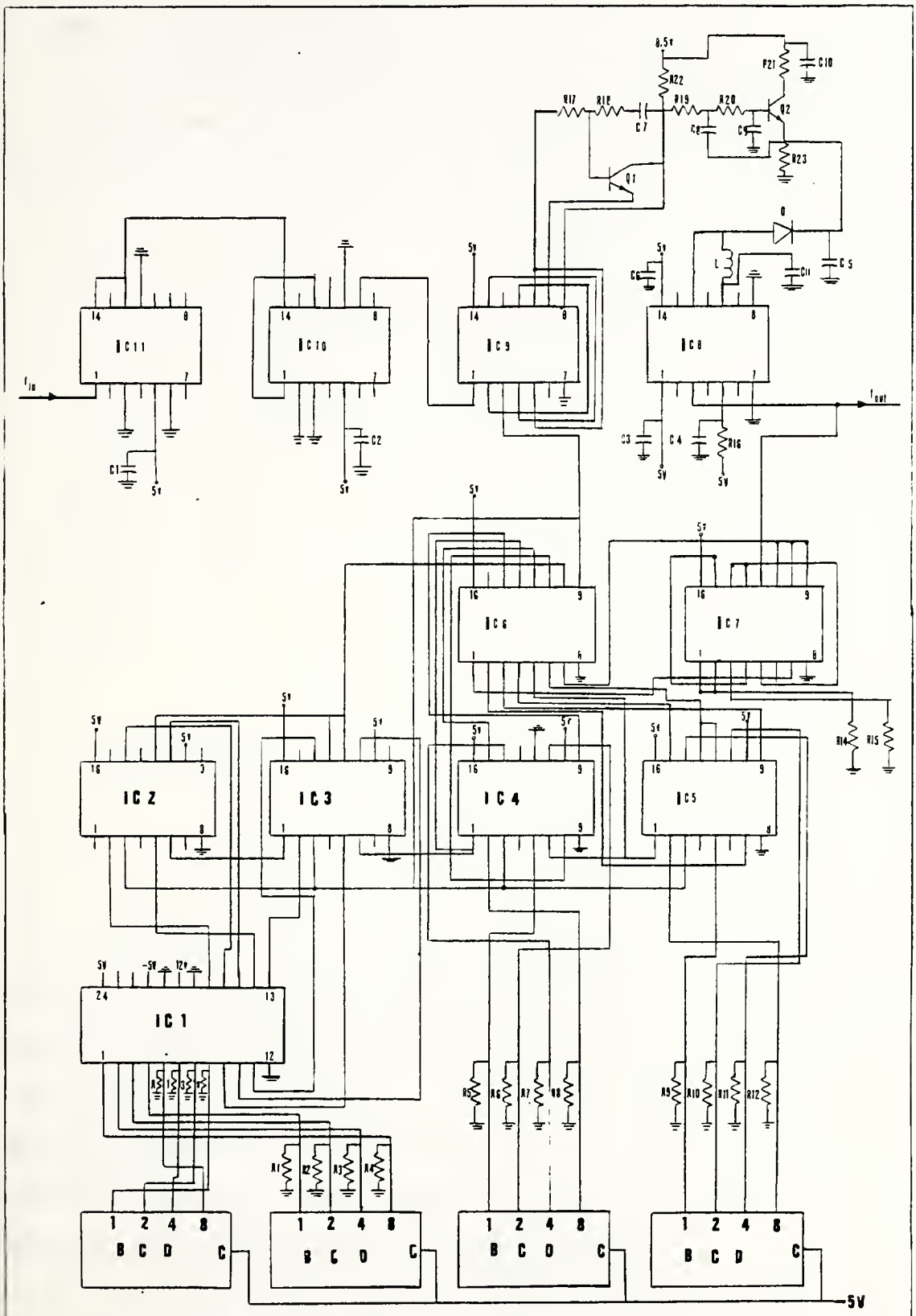


FIGURE 21 COMPLETE SCHEMATIC

V. SUMMARY OF PERFORMANCE CHARACTERISTICS

Performance characteristics of the PLL synthesizer are summarized as follows:

Frequency Range:	47.5 MHz to 97.5 MHz
Frequency Selection:	Electronically tuned
Channel Spacing:	25 kHz
Number of discrete frequencies:	2000
Output waveform:	Sinusoidal wave
Frequency stability:	$\pm$ 0.0018%
Lock up time:	4.5 msec
Spurious level:	16 dB at 47.5 MHz 14 dB at 72.5 MHz 16 dB at 97.5 MHz
Power supply requirements:	+5 Volt at 500 ma -5 Volt at 500 ma +12 Volt at 10 ma +8.5 Volt at 10 ma

A sample of the synthesizer output waveform is shown in Figure 22. It was observed by using a Hewlett-Packard 1741A oscilloscope. Figure 23 shows the 25 kHz reference signal and Figure 24 is the output of the programmable counter. Spurious outputs were measured using a Tektronix Type 491 spectrum analyzer. Photographs of the output spectrum are shown in Figure 25, Figure 26 and Figure 27.

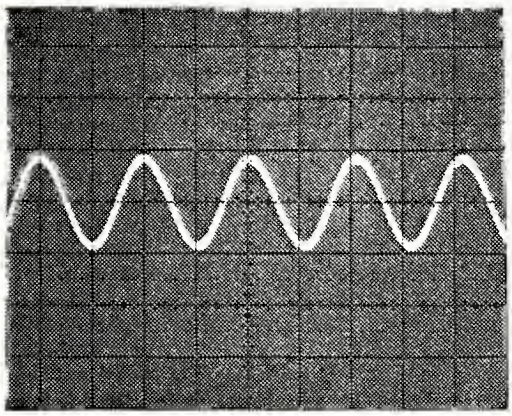


Figure 22. PHOTOGRAPH OF THE PLL OUTPUT VOLTAGE
Vertical Scale: 0.5 V/cm
Horizontal Scale: 0.5 μsec/cm

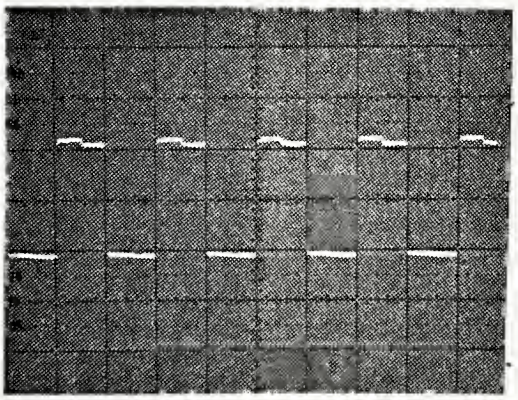


Figure 23. PHOTOGRAPH OF THE REFERENCE FREQUENCY VOLTAGE
Vertical Scale: 2 V/cm
Horizontal Scale: 20 μsec/cm

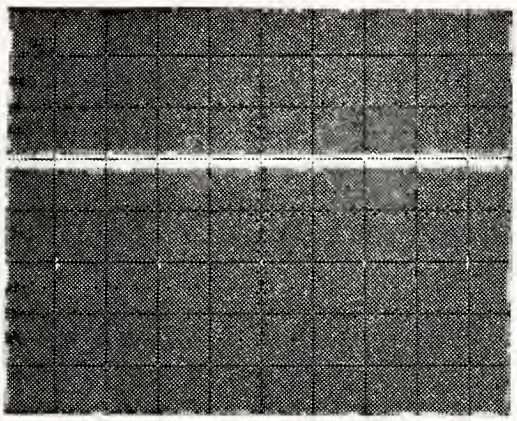
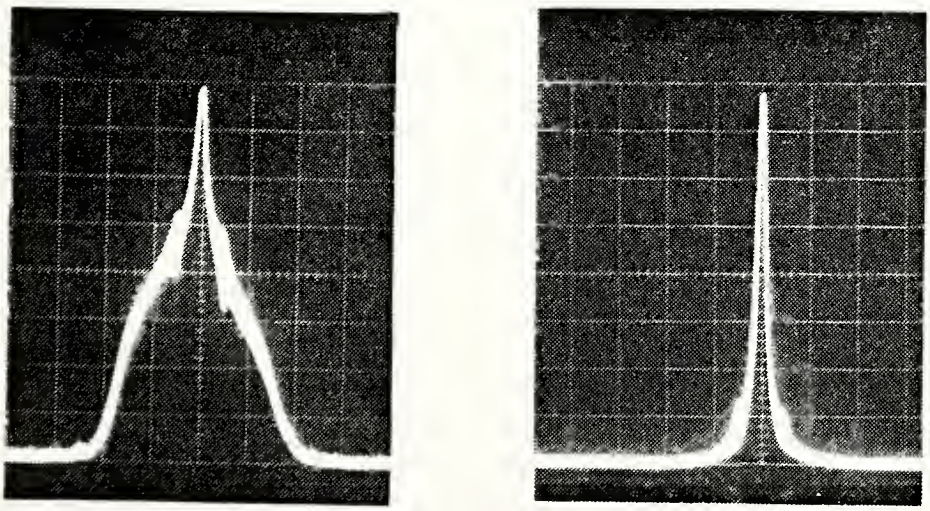


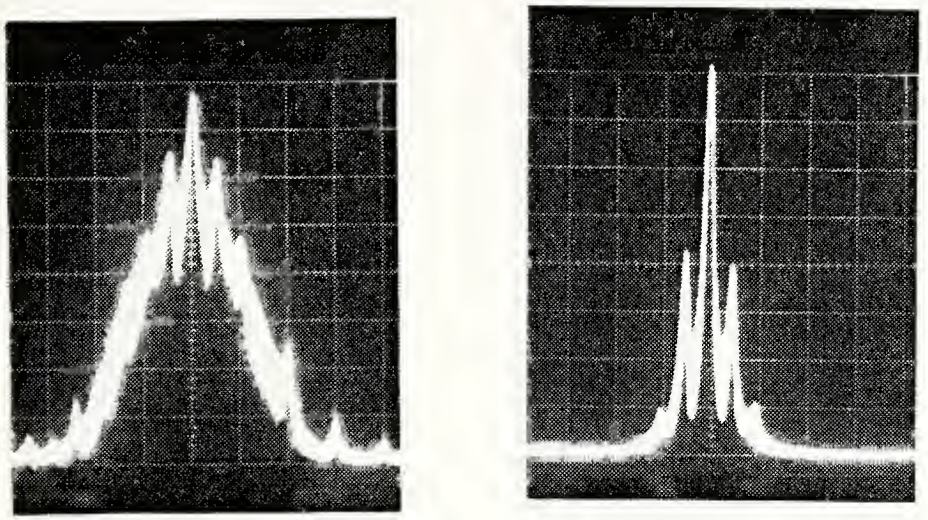
Figure 24. PHOTOGRAPH OF THE PROGRAMMABLE COUNTER OUTPUT VOLTAGE
Vertical Scale: 2 V/cm
Horizontal Scale: 20 μsec/cm



(a)
Dispersion: 50 kHz
Vertical Scale: uncalibrated
Logarithmic Scale

(b)
Dispersion: 50 kHz
Vertical Scale: uncalibrated
Linear Scale

Figure 25. PHOTOGRAPHS OF THE SPECTRUM OF THE PLL OUTPUT VOLTAGE AT 47.5 MHz



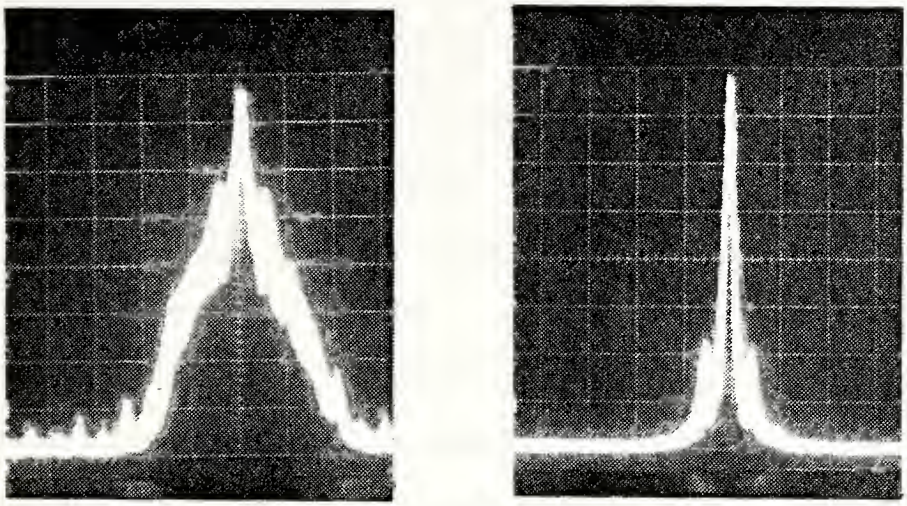
(a)

Dispersion: 50 kHz
Vertical Scale: uncalibrated
Logarithmic Scale

(b)

Dispersion: 50 kHz
Vertical Scale: uncalibrated
Linear Scale

Figure 26. PHOTOGRAPHS OF THE SPECTRUM OF THE PLL OUTPUT VOLTAGE WHEN f_{out} = 72.5 MHz



(a)

Dispersion: 50 kHz
Vertical Scale: uncalibrated
Logarithmic Scale

(b)

Dispersion: 50 kHz
Vertical Scale: uncalibrated
Linear Scale

Figure 27. PHOTOGRAPHS OF THE SPECTRUM OF THE PLL OUTPUT VOLTAGE WHEN f_{out} = 97.5 MHz

VI. SUMMARY AND CONCLUSIONS

A phase-lock loop (PLL) synthesizer suitable for use as the local oscillator in a receiver was designed, built, and tested. It was found from the tests made that the synthesizer would operate properly over the design frequency range of 47.5 MHz to 97.5 MHz in incremental steps of 25 kHz. Switching time from one step to the next is sufficiently fast for the intended purpose. While Figures 25 through 27 show a rather high level of spurious frequencies clustered about the desired frequency it is felt that with some additional engineering and packaging effort the level of these spurious frequencies could be dropped to -40 dB or better below the desired signal. On the average, over the desired tuning range, the spurious frequency level was about -15 dB as the circuit is presently configured. The building and testing phases of this work already show that proper grounding and a stable reference frequency are essential to a successful PLL synthesizer design.

From the experimental results of this thesis, it is concluded that a phase-lock loop synthesizer operating in the desired frequency range can be developed with the characteristics required for use as a local oscillator in a receiver.

APPENDIX A

Component List

Schematic Symbol Number	Description
Resistors	
R1,2,3,4,5,6,7,8,9,10,11,12,13	200 ohms (1/4 Watt)
R14,15	510 ohms (1/4 Watt)
R16,22	1000 ohms (1/4 Watt)
R17	1500 ohms (1/4 Watt)
R18	2000 ohms (1/4 Watt)
R19,20	2700 ohms (1/4 Watt)
R21	1200 ohms (1/4 Watt)
R23	5000 ohms (1/4 Watt)
Capacitors	
C1,2,3,4,5,6	0.1 μF
C7	0.47 μF
C8	1 pF
C9	0.2 μF
C10	1.01 μF
C11	0.1 μF
Inductor	
L	0.11 μH

Diode

D	MV1404

Transistors

Q1,2	2N5089

Integrated Circuits

IC1	CS2708
IC2,3,4,5	MC4016
IC6	MC12014
IC7	MC12012
IC8	MC1648
IC9	MC4044
IC10	74LS93
IC11	74LS90

LIST OF REFERENCES

1. Jon DeLaune, MTTL and MECL Avionic's Digital Frequency Synthesizer, Motorola Semiconductor Products Inc., Application Note AN-532A.

2. Gart Nash, Phase-Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., Application Note AN-535.

3. Applications Engineering, Epicap Tuning Diode Theory and Application, Motorola Semiconductor Products Inc.

4. Dick Brubaker, An ADF Frequency Synthesizer Utilizing Phase-Lock-Loop I/C's, Motorola Semiconductor Products Inc.

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